REMARKS

In the Office Action, the examiner objected to the drawings on the ground that Figures 1A-1D and Figures 2A-2D are not designated by a prior art legend. Accordingly, the applicant has submitted concurrently herewith a request for approval of drawing changes in which a "Prior Art" legend is added to Figures 1A-1D and Figures 2A-2D. Replacement sheets of the drawing are also submitted. Therefore, the applicant believes that the objection to the drawings is no longer applicable to the present invention.

The examiner rejected Claim 3 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. It is stated that the claimed languages "through the host computer in a timely fashion with a minimal time latency and with high priority" are not positive limitation. Accordingly, the applicant has amended Claim 3 to more clearly define the feature of the present invention. Therefore, the applicant believes that the rejection under 35 U.S.C. 112, second paragraph, is no longer applicable to the present invention.

In the Office Action, the examiner rejected Claims 1-12 under 35 U.S.C. 103(a) as being obvious over the technology disclosed by the cited Rhodes reference (U.S. Patent No. 5,557,559). The applicant has amended the claims to more clearly differentiate the present invention from the teachings in the cited Rhodes reference.

The applicant has reviewed very carefully the cited Rhodes reference and is confidant that the structure and method of the semiconductor testing described in the instant application cannot be obvious to anyone skilled in the art.

It should be noted that the cited Rhodes reference is directed to the burn-in test sequence which is fundamentally different from the semiconductor device manufacturing test such as a functional test conducted by the semiconductor test system of the present invention. The structure and operation of the semiconductor test system for the functional test of the semiconductor device is fundamentally different from that of the burn-in testing. As noted by the examiner, the major contribution of the cited Rhodes reference is to provide a graphical interactive means for efficient system set-up; which is unrelated to the present invention. A graphical interactive method for user defined parameters can be developed and used with the test system of the present invention to enhance the efficiency and flexibility to users, but not the point of the present invention.

The examiner has also noted and highlighted that the method in the cited Rhodes reference allows the user to change DUT stress based upon time, temperature or how many times it is run, using a graphical sequence editor. It should be noted that the phrase "time" in the cited patent is "burn-in time" and "sequence" is "temperature and/or voltage stress sequence"; there is no equivalence of this in our application. As known in the art, burn-

in test is to test a life of semiconductor device by heating the semiconductor devices in a heat chamber for several hours. This is not the time critical sequence of the present invention where hundred microseconds of timing resolution must be controlled.

The present application describes a method to define and generate a time critical sequence of operation in a semiconductor test system when the semiconductor test system uses a general purpose operating system. The background section and Figures 1 and 2 in the application describe such time critical operation of the test system. An example includes power on/off, test signal voltage change, time improper power on/off to a certain section of an IC such as a microprocessor or a system-on-a-chip (SoC) can cause whole test to fail.

To detect a manufacturing defect in semiconductor integrated circuits (ICs), the semiconductor test system applies a predetermined value at the input of IC (test vector), obtain response from the IC, and the test system compares the response with an expected value to determine a pass/fail of the IC. This testing process occurs at the functional speed of IC (functional test) or at a predetermined speed when an specialized test structure is used such as scan or built-in self-test. In this test process, sometime a time critical sequence of operation is required to be performed by the semiconductor test system. Often high-speed microprocessors and SoC require such time critical operation for being tested. Time criticality arises because of the high speed of

testing, for example, in today's technology, functional test of an IC can be on the order of GHz.

As described in the background section of our application, one may utilize a special purpose real time tester operating system to define and generate such time critical operation. The present invention employs the method and structure to define and generate the time critical sequence when the semiconductor test system utilizes a general purpose operating system (such as Microsoft Windows). Examiner has correctly noted that there is no equivalence of such structure in the cited Rhodes reference.

It should be noted that the claimed invention specifies that the computing of configuration data and timing data is based on the test program prior to testing the DUT, there is no notion of interactive means as described in the cited Rhodes reference. The claimed invention also specifies the use of the general purpose operating system and a hardware means to generate time critical triggers at a predetermined time defined by the device driver, there is no notion or equivalence of this structure in the cited Rhodes reference.

The applicant has amended Claims 1 and 8 to more clearly specify the relationship among the host computer using the general-purpose operating system, the device driver, and the hardware timer when an interrupt signal is generated. Namely, the host computer transfers the interrupt signal from the hardware timer to the device driver, and the device driver causes to start the test

pattern upon receiving the interrupt signal from the hardware timer through the host computer and to deactivate the power sources to the DUT upon receiving the interrupt signal from the hardware timer through the host computer. The cited Rhodes reference does not show or suggest such features of the present invention.

As discussed above, the present invention is not obvious over the cited Rhodes reference, and thus, Applicant believes that the rejection under 35 U.S.C. 103(a) is no longer applicable to the present invention.

In this opportunity, Applicant has amended the specification to correct the minor errors therein and to more clearly disclose the present invention. This is to verify that no new matter has been introduced by this amendment.

In view of the foregoing, Applicant believes that Claims 1-52 are in condition for allowance, and accordingly, Applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

MURAMATSU & ASSOCIATES

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By: _____

Yasuo Muramatsu
Registration No. 38,684
Attorney of Record
7700 Irvine Center Drive
Suite 225, Irvine, CA 92618
(949) 753-1127

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Prior Art

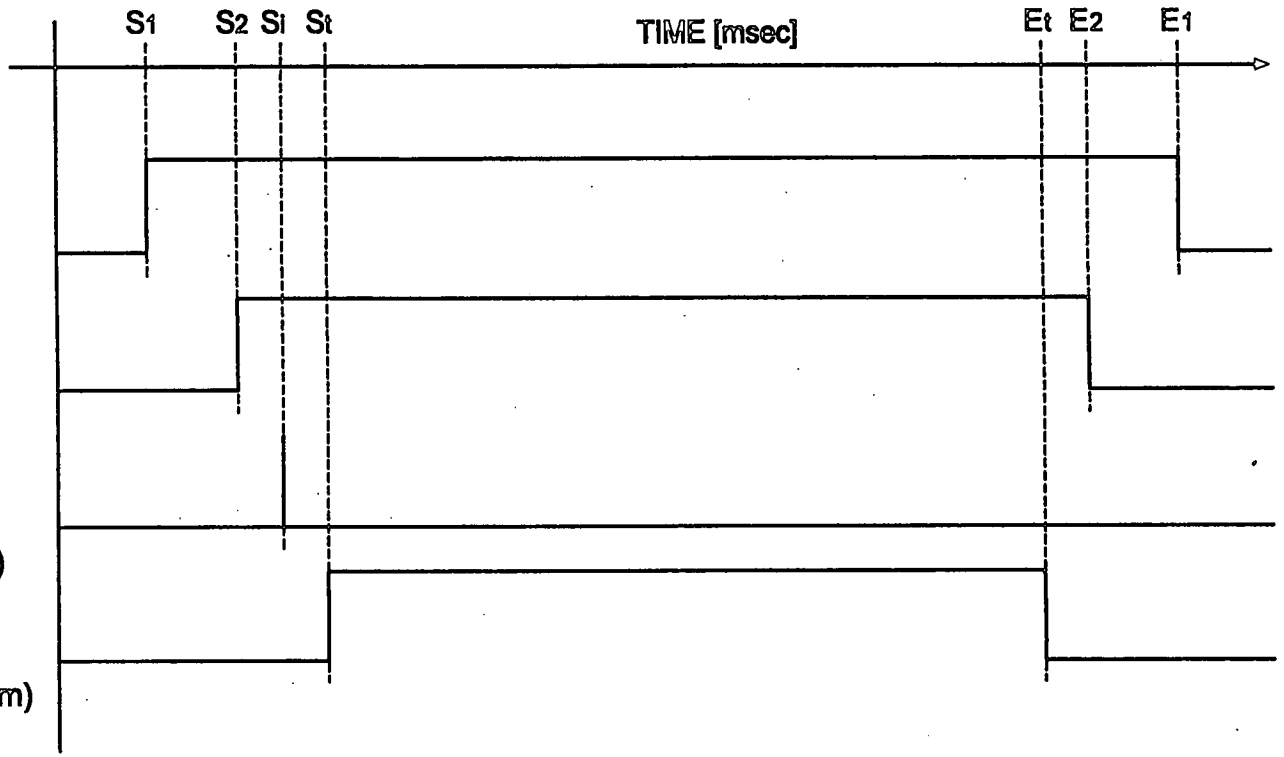

Fig. 1A
(DUT Power #1)

Fig. 1B
(DUT Power #2)

Fig. 1C
(DUT Initialization)

Fig. 1D
(Digital Test Pattern)

Prior Art

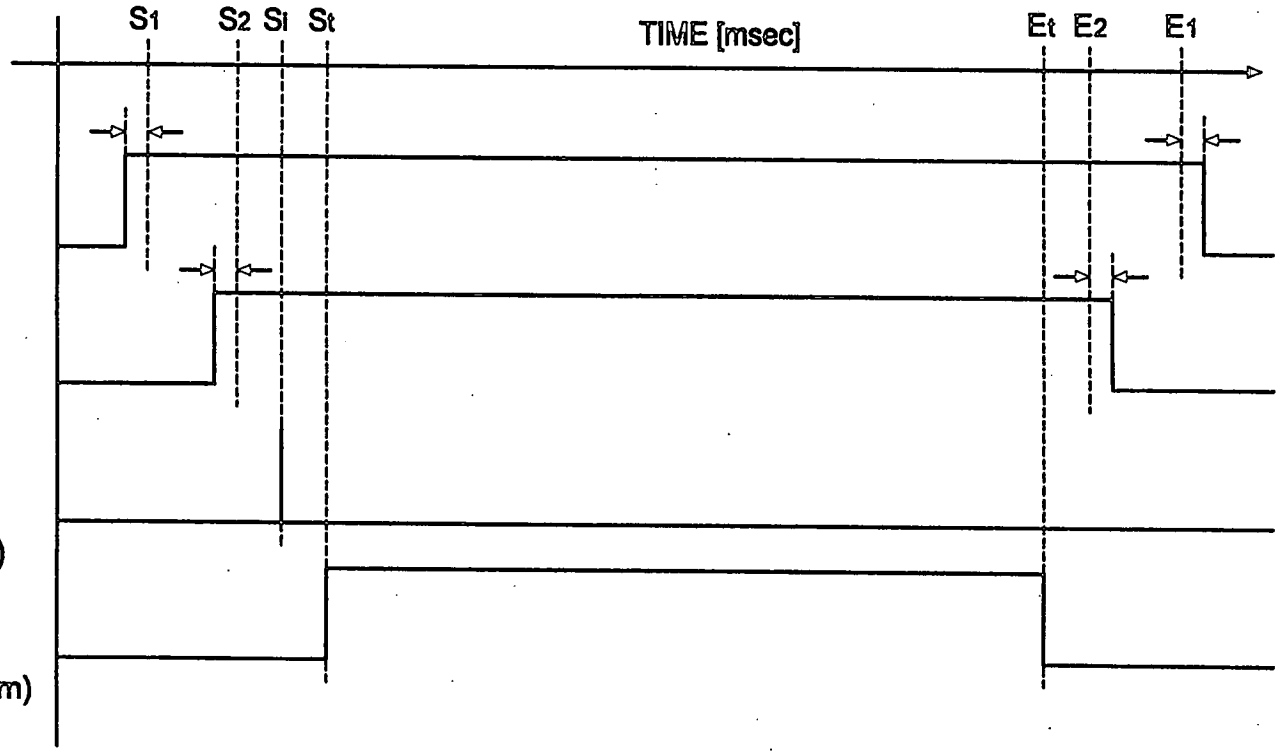

Fig. 2A
(DUT Power #1)

Fig. 2B
(DUT Power #2)

Fig. 2C
(DUT Initialization)

Fig. 2D
(Digital Test Pattern)